

3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED:
 $t_{PD} = 5.5\text{ns}$ (TYP.) at $V_{CC} = 3.3\text{V}$
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:
 $I_{CC} = 4\ \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- LOW NOISE:
 $V_{OLP} = 0.2\text{V}$ (TYP.) at $V_{CC} = 3.3\text{V}$
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 12\text{mA}$ (MIN) at $V_{CC} = 3.0\text{V}$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 2\text{V}$ to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 138
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74LVQ138 is a low voltage CMOS 3 TO 8 LINE DECODER (INVERTING) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and low noise 3.3V applications.



Table 1: Order Codes

| PACKAGE | T & R |
|---------|-------------|
| SOP | 74LVQ138MTR |
| TSSOP | 74LVQ138TTR |

If the device is enabled, 3 binary select inputs (A, B, and C) determine which one of the outputs will go low. If enable input G1 is held low or either G2A or G2B is held high, the decoding function is inhibited and all the 8 outputs go to high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

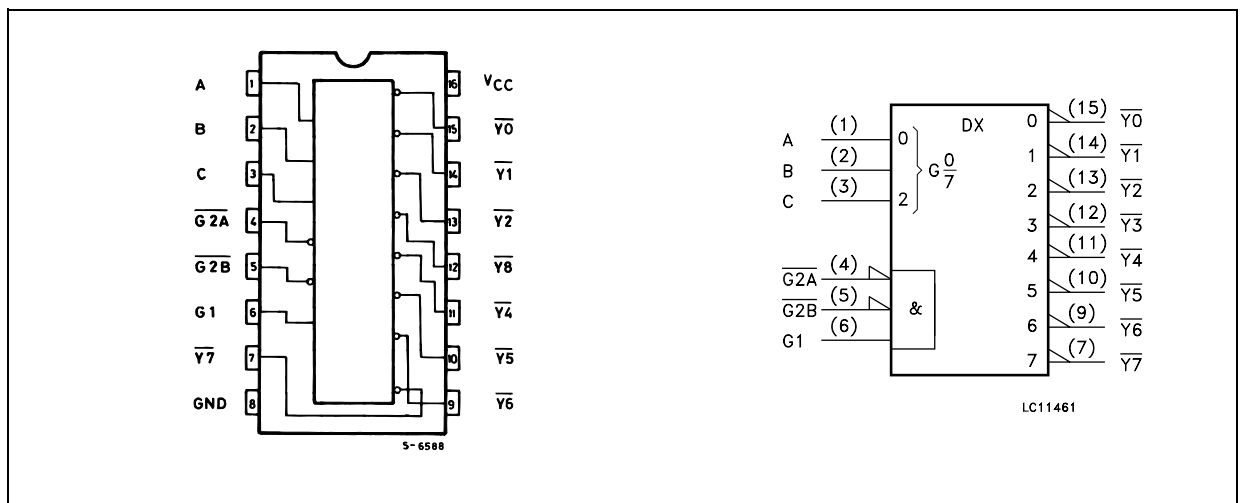


Figure 2: Input And Output Equivalent Circuit

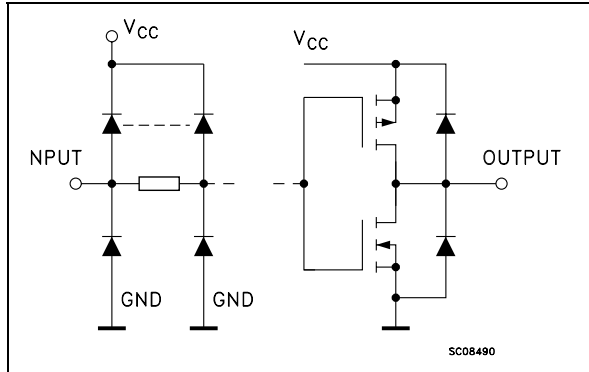


Table 2: Pin Description

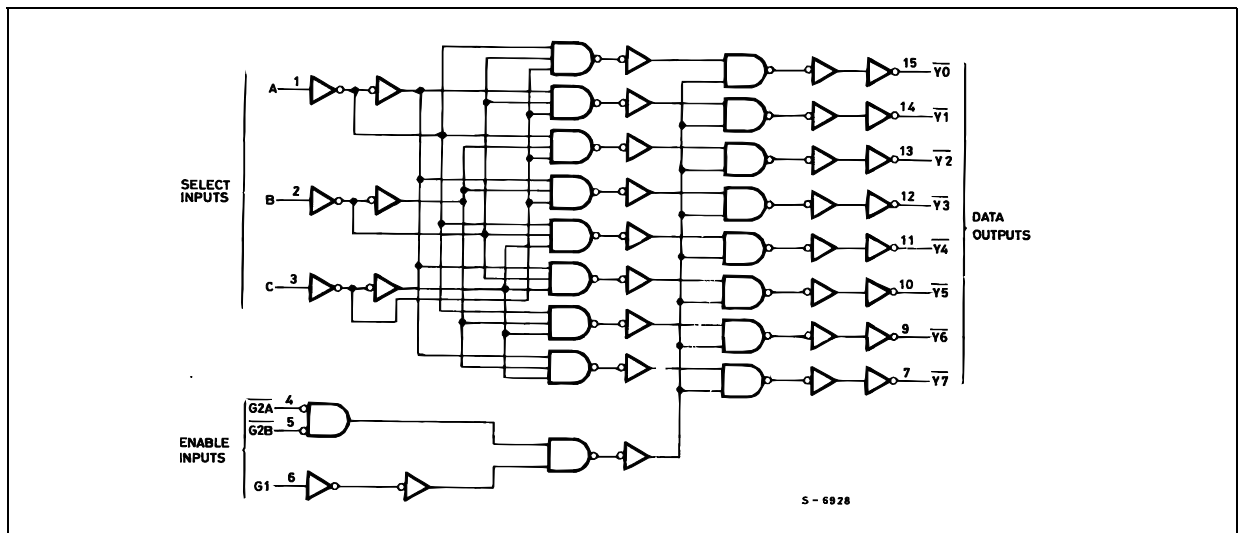
| PIN N° | SYMBOL | NAME AND FUNCTION |
|------------------------------|-----------------|-------------------------|
| 1, 2, 3 | A, B, C | Address Inputs |
| 4, 5 | G2A, G2B | Enable Inputs |
| 6 | G1 | Enable Input |
| 15, 14, 13, 12, 11, 10, 9, 7 | Y0 to Y7 | Outputs |
| 8 | GND | Ground (0V) |
| 16 | V _{CC} | Positive Supply Voltage |

Table 3: Truth Table

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|------------------|------------------|----|--------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| ENABLE | | | SELECT | | | | | | | | | | |
| $\overline{G2B}$ | $\overline{G2A}$ | G1 | C | B | A | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not been used to estimate propagation delays

Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-----------------------|-------------------------------|------------------------|------|
| V_{CC} | Supply Voltage | -0.5 to +7 | V |
| V_I | DC Input Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 20 | mA |
| I_O | DC Output Current | ± 50 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 200 | mA |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5: Recommended Operating Conditions

| Symbol | Parameter | Value | Unit |
|----------|---|---------------|------|
| V_{CC} | Supply Voltage (note 1) | 2 to 3.6 | V |
| V_I | Input Voltage | 0 to V_{CC} | V |
| V_O | Output Voltage | 0 to V_{CC} | V |
| T_{op} | Operating Temperature | -55 to 125 | °C |
| dt/dv | Input Rise and Fall Time $V_{CC} = 3.0V$ (note 2) | 0 to 10 | ns/V |

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2V

Table 6: DC Specifications

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------|------------------------------------|-----------------|-------------------------------|--------------------------|-------|-----------|-------------|---------|--------------|---------|---------------|
| | | V_{CC} (V) | | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V_{IH} | High Level Input Voltage | 3.0 to 3.6 | | 2.0 | | | 2.0 | | 2.0 | | V |
| V_{IL} | Low Level Input Voltage | | | | 0.8 | | 0.8 | | 0.8 | | V |
| V_{OH} | High Level Output Voltage | 3.0 | $I_O = -50 \mu\text{A}$ | 2.9 | 2.99 | | 2.9 | | 2.9 | | V |
| | | | $I_O = -12 \text{ mA}$ | 2.58 | | | 2.48 | | 2.48 | | |
| | | | $I_O = -24 \text{ mA}$ | | | | 2.2 | | 2.2 | | |
| V_{OL} | Low Level Output Voltage | 3.0 | $I_O = 50 \mu\text{A}$ | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | $I_O = 12 \text{ mA}$ | | 0 | 0.36 | | 0.44 | | 0.44 | |
| | | | $I_O = 24 \text{ mA}$ | | | | | 0.55 | | 0.55 | |
| I_I | Input Leakage Current | 3.6 | $V_I = V_{CC}$ or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I_{CC} | Quiescent Supply Current | 3.6 | $V_I = V_{CC}$ or GND | | | 4 | | 40 | | 40 | μA |
| I_{OLD} | Dynamic Output Current (note 1, 2) | 3.6 | $V_{OLD} = 0.8 \text{ V max}$ | | | | 36 | | 25 | | mA |
| I_{OHD} | | | $V_{OHD} = 2 \text{ V min}$ | | | | -25 | | -25 | | mA |

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75Ω

Table 7: Dynamic Switching Characteristics

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|------------------|--|------------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{OLP} | Dynamic Low Voltage Quiet Output (note 1, 2) | 3.3 | C _L = 50 pF | | 0.2 | 0.8 | | | | | V |
| V _{OLV} | | | | -0.8 | -0.2 | | | | | | |
| V _{IHD} | Dynamic High Voltage Input (note 1, 3) | 3.3 | | 2 | | | | | | V | |
| V _{ILD} | Dynamic Low Voltage Input (note 1, 3) | 3.3 | | | | 0.8 | | | | | V |

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|--|--|------------------------|--|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| t _{PLH} t _{PHL} | Propagation Delay Time A, B, C to \bar{Y} | 2.7 | | | 6.6 | 10.5 | | 12.0 | | 14.0 | ns |
| | | 3.3 ^(*) | | | 5.5 | 8.0 | | 9.0 | | 10.5 | |
| t _{PLH} t _{PHL} | Propagation Delay Time G1 to Y | 2.7 | | | 6.7 | 10.5 | | 12.0 | | 14.0 | ns |
| | | 3.3 ^(*) | | | 5.6 | 8.0 | | 9.0 | | 10.5 | |
| t _{PLH} t _{PHL} | Propagation Delay Time G2A or $\overline{G2B}$ to \bar{Y} | 2.7 | | | 6.3 | 10.5 | | 12.0 | | 14.0 | ns |
| | | 3.3 ^(*) | | | 5.2 | 8.0 | | 9.0 | | 10.5 | |
| t _{OSLH} t _{OSHL} | Output To Output Skew Time (note1, 2) | 2.7 | | | 0.5 | 1.0 | | 1.0 | | 1.0 | ns |
| | | 3.3 ^(*) | | | 0.5 | 1.0 | | 1.0 | | 1.0 | |

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)

2) Parameter guaranteed by design

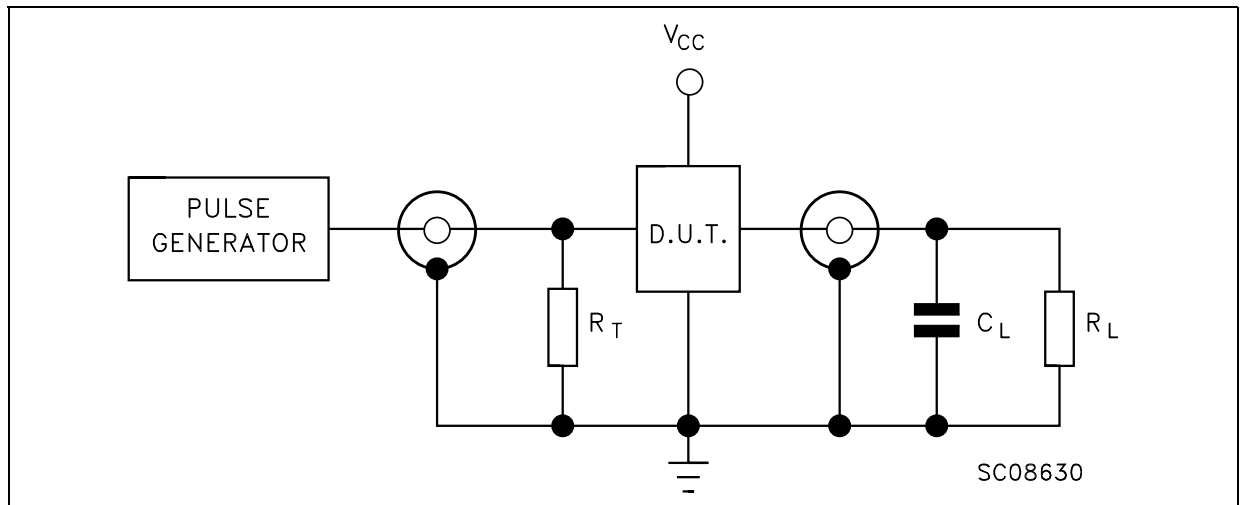
(*) Voltage range is 3.3V ± 0.3V

Table 9: Capacitive Characteristics

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------------|--|------------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C _{IN} | Input Capacitance | 3.3 | | | 4 | | | | | | pF |
| C _{PD} | Power Dissipation Capacitance (note 1) | 3.3 | f _{IN} = 10MH | | 50 | | | | | | pF |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}

Figure 4: Test Circuit



C_L = 50pF or equivalent (includes jig and probe capacitance)

R_L = 500 Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50 Ω)

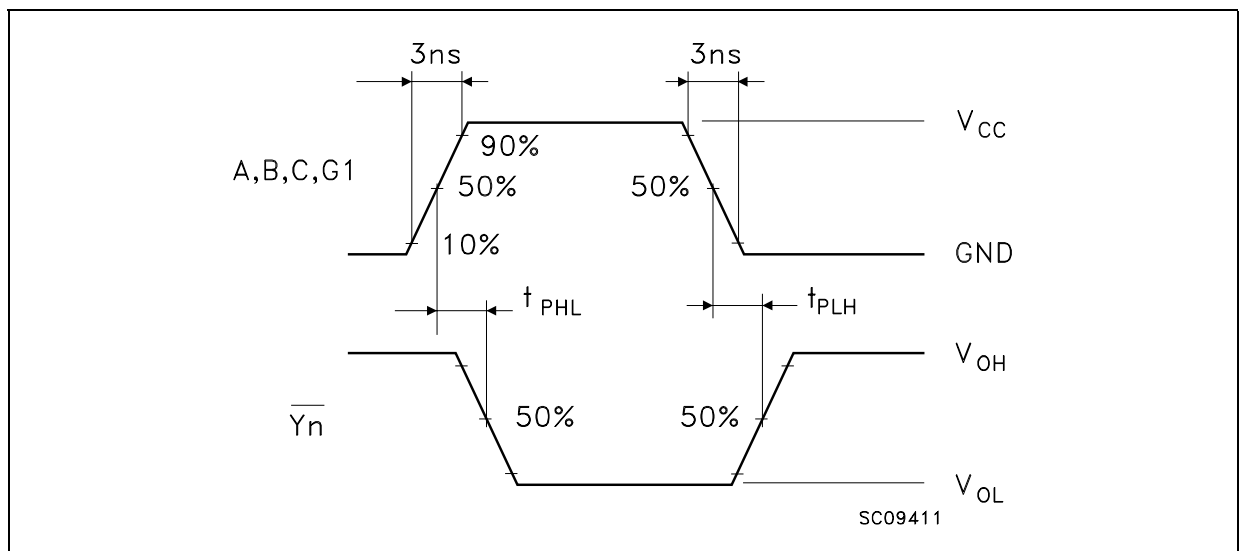
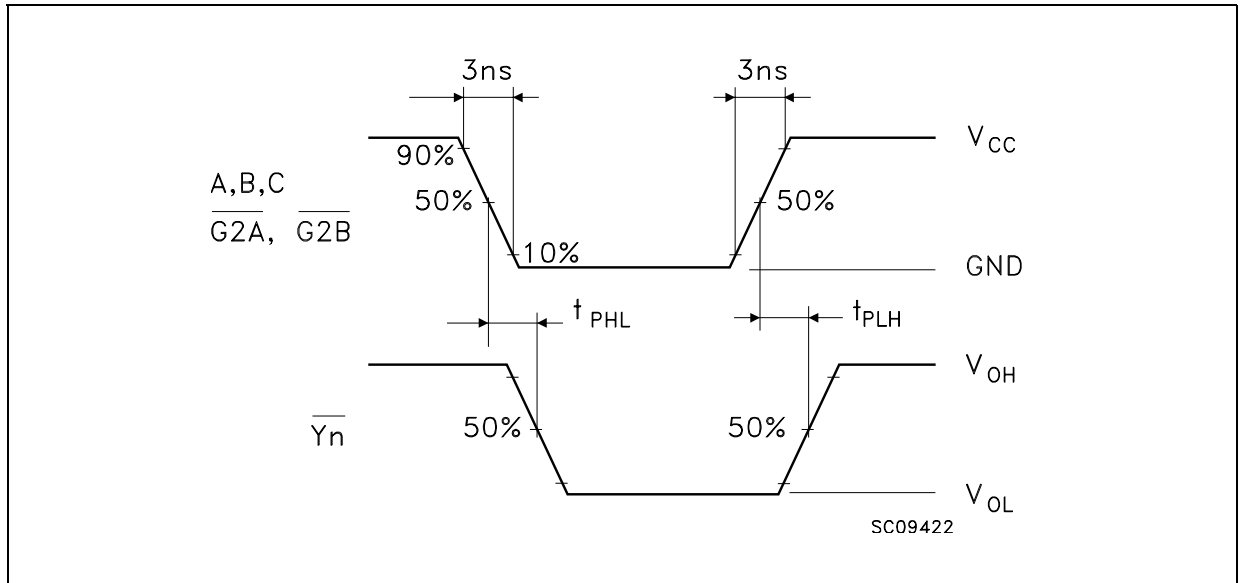
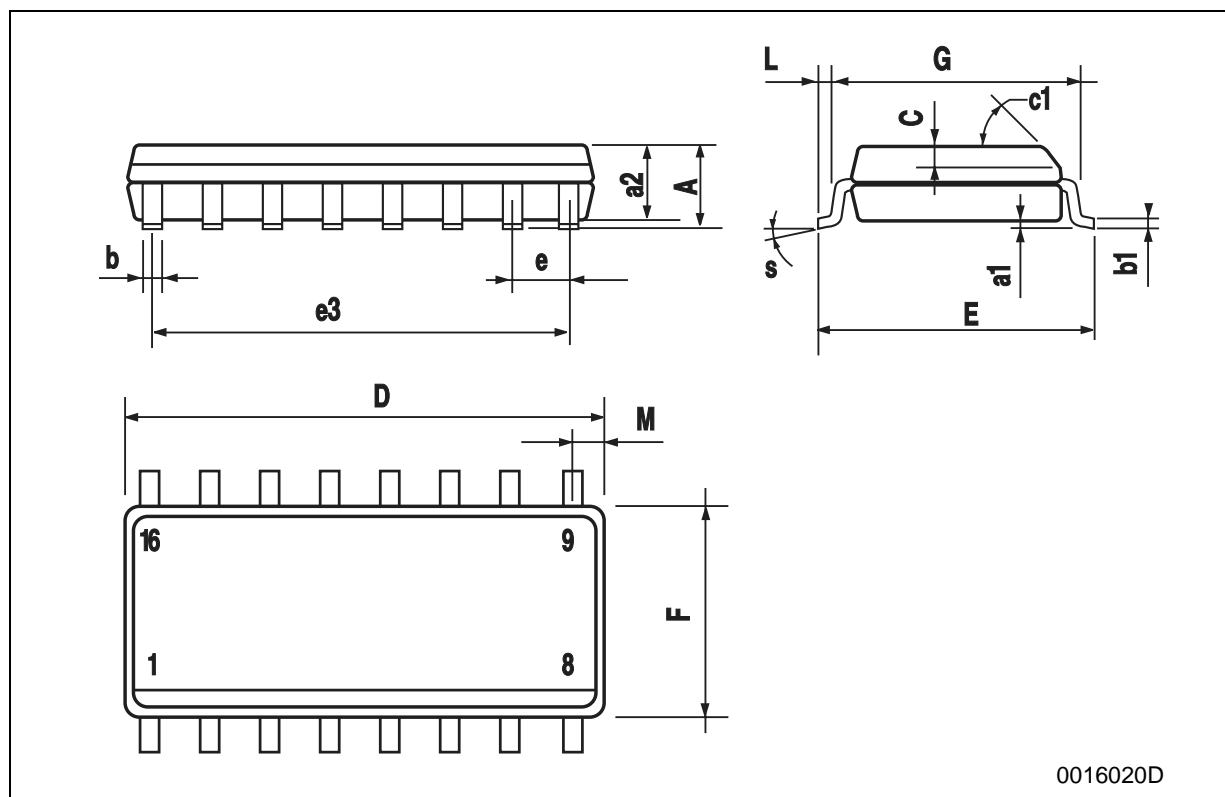
Figure 5: Waveform - Propagation Delays For Inverting Outputs ($f=1\text{MHz}$; 50% duty cycle)

Figure 6: Waveform - Propagation Delays For Non-inverting Outputs ($f=1\text{MHz}$; 50% duty cycle)

SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.64 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |



TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0079 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



0080338D

Tape & Reel SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.45 | | 6.65 | 0.254 | | 0.262 |
| Bo | 10.3 | | 10.5 | 0.406 | | 0.414 |
| Ko | 2.1 | | 2.3 | 0.082 | | 0.090 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



Tape & Reel TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.7 | | 6.9 | 0.264 | | 0.272 |
| Bo | 5.3 | | 5.5 | 0.209 | | 0.217 |
| Ko | 1.6 | | 1.8 | 0.063 | | 0.071 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



Table 10: Revision History

| Date | Revision | Description of Changes |
|-------------|----------|-----------------------------------|
| 29-Jul-2004 | 5 | Ordering Codes Revision - pag. 1. |

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